IN THE CLAIMS

Please cancel claims 1-40 and add the following new claims 41-65 as follows:

1-40. (Cancelled)

41. (New) A packaged semiconductor device comprising:

a plurality of external connectors for a semiconductor package;

a system chip disposed within the semiconductor package and connected to at least a portion of said plurality of external connectors for communicating with a component external to the semiconductor package during a normal mode of operation; and

a memory chip disposed within the semiconductor package and connected to said system chip through a data bus, said memory chip comprising:

a plurality of data buffers for transferring data between said memory chip and said system chip through said data bus during the normal mode of operation; and

at least one test buffer directly connected to certain of said portion group of said plurality of external connectors through a path not including the data bus to provide testing of said memory chip during a test mode of operation and while contained within the semiconductor package.

42. (New) The packaged semiconductor device of Claim 41 wherein said memory chip comprises at least one of a random access memory (RAM), a static RAM, a dynamic RAM, a non-volatile RAM, a read only memory (ROM), a programmable ROM, an erasable programmable ROM, an electrically erasable programmable ROM, and a flash memory.

43. (New) The packaged semiconductor device of Claim 41 wherein said system chip comprises at least one of a processor, a microcontroller (ASIC), a microprocessor, a field programmable gate array, and an application specific integrated circuit.

44. (New) The packaged semiconductor device of Claim 41 wherein said memory chip comprises at least an eight bit dynamic random access memory which communicates with said system chip through said data bus having a bus width equal to or greater than the number of bits of said memory chip.

45. (New) The packaged semiconductor device of Claim 44 wherein said data bus has a bus width of at least 32 bits.

46. (New) The packaged semiconductor device of Claim 41 wherein said at least one test buffer provides data compression.

47. (New) The packaged semiconductor device of Claim 41 wherein a ratio of said data buffers to said at least one test buffer is greater than or equal to 2:1.

48. (New) The packaged semiconductor device of Claim 41 wherein said at least one test buffer is disabled during the normal mode of operation and enabled during the test mode of operation, wherein said at least one test buffer provides said memory chip with signals for at least one of addresses, control, and data.

49. (New) The packaged semiconductor device of Claim 41 wherein said at least one test buffer communicates with external memory test equipment through said certain of said portion of said plurality of external connectors to test said memory chip.

50. (New) The packaged semiconductor device of Claim 41 wherein at least one of said plurality of data buffers incorporates said at least one test buffer.

51. (New) A semiconductor memory chip for packaging along with a system chip in a single semiconductor package having a plurality of external connectors, the memory chip comprising:

a memory storage array for storing data;

a plurality of data buffers for writing or reading data between said memory storage array and the system chip within the single semiconductor package; and

at least one test buffer directly connected to certain of said plurality of external connectors for supporting testing of said memory chip within the single semiconductor package by external test equipment.

52. (New) The memory chip of Claim 51 wherein said memory chip comprises at least one of a random access memory (RAM), a static RAM, a dynamic RAM, a non-volatile RAM, a read only memory (ROM), a programmable ROM, an erasable programmable ROM, an electrically erasable programmable ROM, and a flash memory.

53. (New) The memory chip of Claim 51 wherein said at least one test buffer provides data compression.

54. (New) The memory chip of Claim 51 wherein said at least one test buffer is disabled during a normal mode of operation and enabled during a test mode of operation, wherein said at least one test buffer provides said memory chip with signals for at least one of addresses, control, and data input.

55. (New) The memory chip of Claim 51 wherein said at least one test buffer communicates with external memory test equipment through the certain of said plurality of external connectors to test said memory chip.

56. (New) The memory chip of Claim 51 wherein at least one of said plurality of data buffers incorporates said at least one test buffer.

57. (New) A packaged semiconductor device comprising:

a plurality of external connectors for a semiconductor package;

a primary chip disposed within the semiconductor package and connected to at least a portion of said plurality of external connectors; and

a secondary chip disposed within the semiconductor package and connected to said primary chip, said secondary chip comprising:

a plurality of data signal drivers for transferring information between said secondary chip and said primary chip during a normal mode of operation; and

at least one test signal driver directly connected to certain of said portion of said plurality of external connectors to provide testing of said secondary chip during a test mode of operation and while contained within the semiconductor package.

58. (New) The packaged semiconductor device of Claim 57 wherein said secondary chip comprises at least one of a memory chip, a co-processor chip, an analog subsystem, and an application-specific subsystem.

59. (New) The packaged semiconductor device of Claim 57 wherein said primary chip comprises at least one of a processor, a microcontroller, a microprocessor, a field programmable gate array, and an application specific integrated circuit (ASIC).

60. (New) The packaged semiconductor device of Claim 57 wherein said at least one test signal driver is operable to compress data.

61. (New) The packaged semiconductor device of Claim 57 wherein said at least one test signal driver is disabled during the normal mode of operation and enabled during the test mode of operation.

62. (New) The packaged semiconductor device of Claim 57 wherein said at least one test signal driver communicates with external test equipment through said certain of said portion of said plurality of external connectors.

63. (New) A semiconductor chip for incorporation as a secondary chip into a multi-chip packaged semiconductor device, the semiconductor chip comprising:

at least one data buffer operable to connect to a primary chip incorporated into the multi-chip packaged semiconductor device for receiving from and outputting signals to the primary chip during a normal mode of operation; and

a test buffer operable to directly connect to an external terminal of the multi-chip packaged semiconductor device for receiving from and outputting signals to external testing circuitry during a test mode of operation.

64. (New) The semiconductor chip of Claim 63 wherein during the test mode of operation, the at least one data buffer is tri-stated and the test buffer is enabled to provide testing for the semiconductor chip.

65. (New) The semiconductor chip of Claim 63 wherein during the normal mode of operation, the at least one data buffer is enabled and the test buffer is tri-stated.